REMARKS

Claims 1-10, 14-29 are currently pending.

Claims 1-5, 10, 14 and 15 are amended. The amendments are being made for clarity and not patentability purposes, and no new matter is being added. Basis for the amendments to Claims 1, 2 and 5 can be found on page 4, lines 11 and 12 of the specification.

In section 1 of the Office Action , Claims 1-7, 9, 14, 15, 17, 20 and 22-27 are rejected under 35 USC § 103(a) as being unpatentable over US patent No. 5,996,057 (hereinafter referred to as "the Scales, III et al. patent") in view of US patent No. 5,758,176 (hereinafter referred to as "the Agarwal patent"). Applicants are traversing this rejection.

The application now contains four independent claims, namely Claims 1, 2, 5 and newly presented Claim 28. Below, Applicants explain that the Scales, III et al. patent does not disclose all of the elements of amended Claims 1, 2, 5, and 28.

As previously explained, the Scales, III et al. patent relates to a data processing system (col. 2, line 59). According to col. 2, lines 60-66 of Scales, III et al. the data processing system allows the specification of 3 input operands comprising 2 input vectors and a control vector. The input operands are loaded into vector registers and a Permute-With- Replication (PWR) operation is performed on the 2 input vectors in a manner specified by the control vector. The result of the PWR operation is stored as an output operand in an output register.

The precise configuration of the data processing system disclosed in Scales, III et al. patent is described further at col. 5, lines 31-48. In particular, col. 5, lines 33-34, the system comprises a vector register file 200 having 32 vector registers. The vector register file 200 is coupled to a combine network 210 (col. 5, lines 35-36). The vector register file 200 provide 3 vectors (A, B and C) from 3 pre-selected or programmed registers of the vector register file 200 (col. 5, lines 36-38). The PWR operation is performed by the combine network 210, and the vector register file 200 includes a control register containing the control vector (col. 5, lines 46-47).

The above system is configured in a manner consistent with the description of FIG. 1 of the present application, which addresses known art.

Claim 1 recites, *inter alia*, the following features:

• a vector register file

• a permutation logic block coupled to receive and permutate vectors from at least one vector register of the vector register file according to control parameters, permutation of the vectors being as a side operation of an instruction;

• a plurality of control registers separate from the vector register file, each of the plurality of control registers being coupled to selectively provide control parameters to the permutation logic block; and

• control means coupled between the plurality of control registers and the permutation logic block and arranged for selecting one of the plurality of control registers and for providing the control parameters from the selected one of the plurality of control registers to the permutation logic block.

The Scales, III et al. patent does not possess separate features of a vector register file and a plurality of control registers as recited in Claim 1. The control vectors of the Scales, III et al. patent are contained in the vector register file 200.

The Agarwal patent describes a single-instruction, multiple data (SIMD) execution unit for use in conjunction with a superscalar data processing system (Abstract). Referring to Figure 4 of the Agarwal patent, a superscalar processor 200 is interfaced with an SIMD execution unit 156. Referring to Figure 5, the SIMD execution unit 156 comprises a plurality of processing elements 230-234 coupled to a control unit 180 via a common command bus 184 and a plurality of individual data buses 186 (col. 7, lines 45-50). The processing elements 230-234 include a register file 236, the register file 236 optionally including 6 parts to allow a load or store operation to take place in parallel with an arithmetic operation. The register file 236 stores operands and results for vector operations performed by the processing elements 230-234 (col. 7, lines 51-57). Col. 8, lines 1-2 state that control registers 244 are included within the processing elements 233-234. Also, other control registers 244 may be used during operations that require indirect addressing of registers in the register file 236.

However, if the skilled person were to combine the teachings of the cited Scales III et al. patent and the Agarwal patent, the resulting combination would fail to teach a plurality of control registers that are separate from a vector register file in combination

with permutation of vectors as a side operation of an instruction according to control parameters provided by the plurality of control registers, as recited in Claim 1.

In view of the reasoning provided above, Applicants submit that Claim 1 is not unpatentable over the cited Scales III et al. patent in view of the Argarwal patent.

Amended Claim 2 provides for a single-instruction multiple-data microprocessor vector permutation system comprising controller coupled between the plurality of control registers, a separate vector register file and the permutation logic block, where the permutation of the vectors is a side operation of an instruction. As explained above in support of Claim 1, the Scales, III et al. patent does not disclose the plurality of control registers being separate from the vector register file in combination with permutation of vectors as a side operation of an instruction, as recited in Claim 2. Accordingly, Claim 2 is considered patentable over the Scales, III et al. patent in view of the Agarwal patent.

Amended Claim 5 provides for a method for permutation in a single-instruction multiple-data microprocessor where a controller is provided between the plurality of control registers, a separate vector register file, and the permutation logic block, where the permutation of the vectors is a side operation of an instruction. As explained above in support of Claim 1, the combined teachings of the Scales, III et al. patent do not teach the plurality of control registers being separate from the vector register file in combination with permutation of vectors as a side operation of an instruction, as recited in Claim 5.

In view of the reasoning provided above, Applicants submit that Claim 5 is patentable over the Scales, III et al. patent in view of the Agarwal patent.

Turning to Claim 28, as stated previously above, Claim 28 incorporates the further feature of the controller including at least one counter arranged to provide a sequential order for cyclically sequencing through the plurality of control registers. In the Office Action, col. 3, lines 11-13 have been cited. However, this statement simply alludes to some form of serial "chain of binary functions". This statement does not disclose sequencing through the plurality of control registers, and moreover in a cyclic manner.

Consequently, the combined teachings of the cited Scales, III et al. patent and the Agarwal patent do not disclose the presence of at least one counter arranged to

provide a sequential order for cyclically sequencing through the plurality of control registers, as recited in Claim 28.

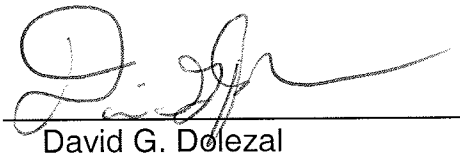
In view of the reasoning provided above, Applicants submit that Claim 28 is patentable over the Scales, III et al. patent in view of the Agarwal patent.

The dependant claims that depend from the independent claims and are allowable for at least this reason.

The case is believed to be in condition for allowance and notice to such effect is respectfully requested. If there is any issue that may be resolved, the Examiner is respectfully requested to telephone the undersigned.

If Applicant has overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 503079, Freescale Semiconductor, Inc.

Respectfully submitted,

By: 

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